FIG.1

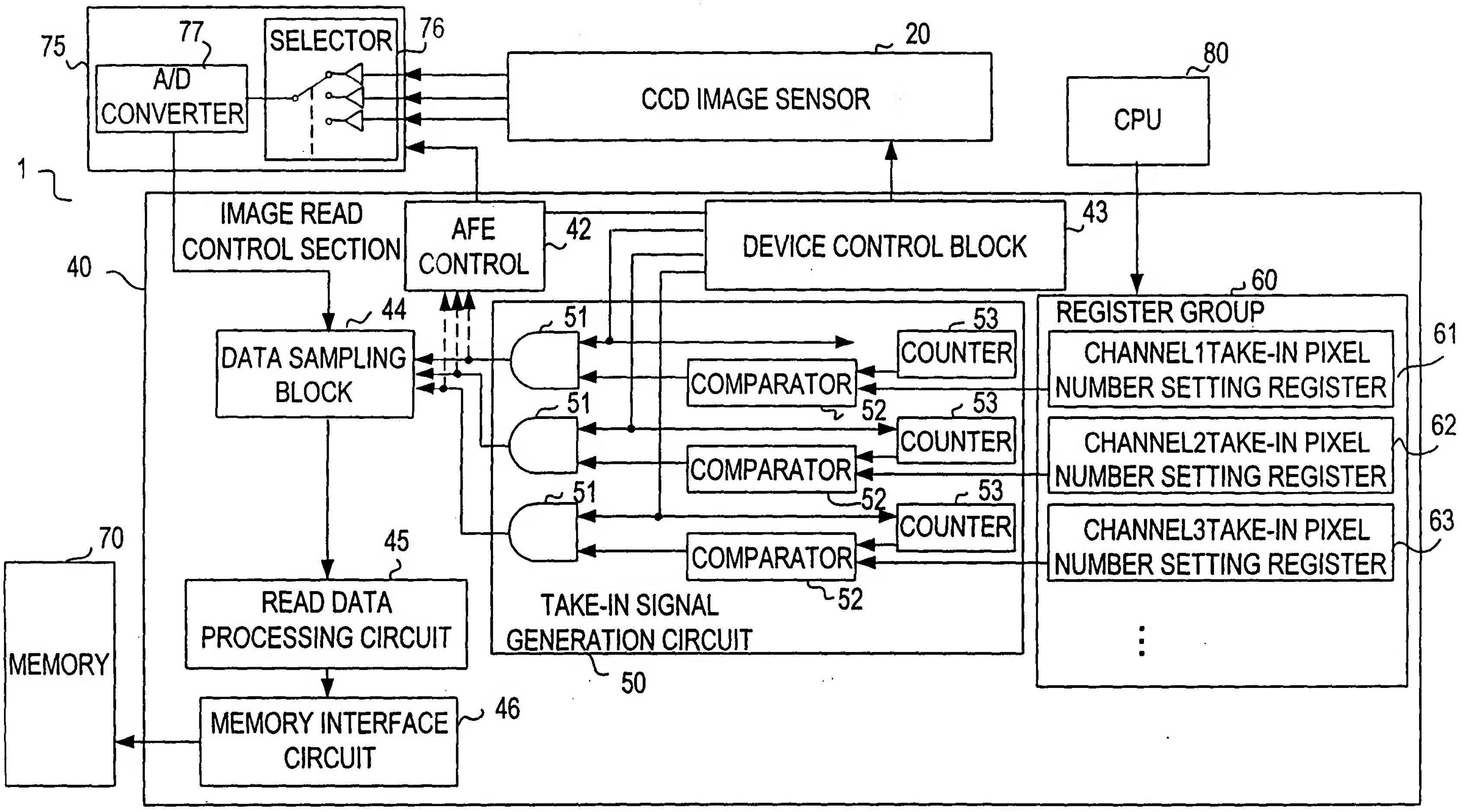

1
75
77
A/D CONVERTER
SELECTOR
76
CCD IMAGE SENSOR
20
CPU
80
40
IMAGE READ CONTROL SECTION
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
60
REGISTER GROUP
CHANNEL1TAKE-IN PIXEL NUMBER SETTING REGISTER
61
CHANNEL2TAKE-IN PIXEL NUMBER SETTING REGISTER
62
CHANNEL3TAKE-IN PIXEL NUMBER SETTING REGISTER
63
⋮
44
DATA SAMPLING BLOCK
51
51
51
COMPARATOR
COMPARATOR
COMPARATOR
52
52
52
COUNTER
COUNTER
COUNTER
53
53
53
TAKE-IN SIGNAL GENERATION CIRCUIT
50
70
MEMORY
45
READ DATA PROCESSING CIRCUIT
MEMORY INTERFACE CIRCUIT
46

FIG.2

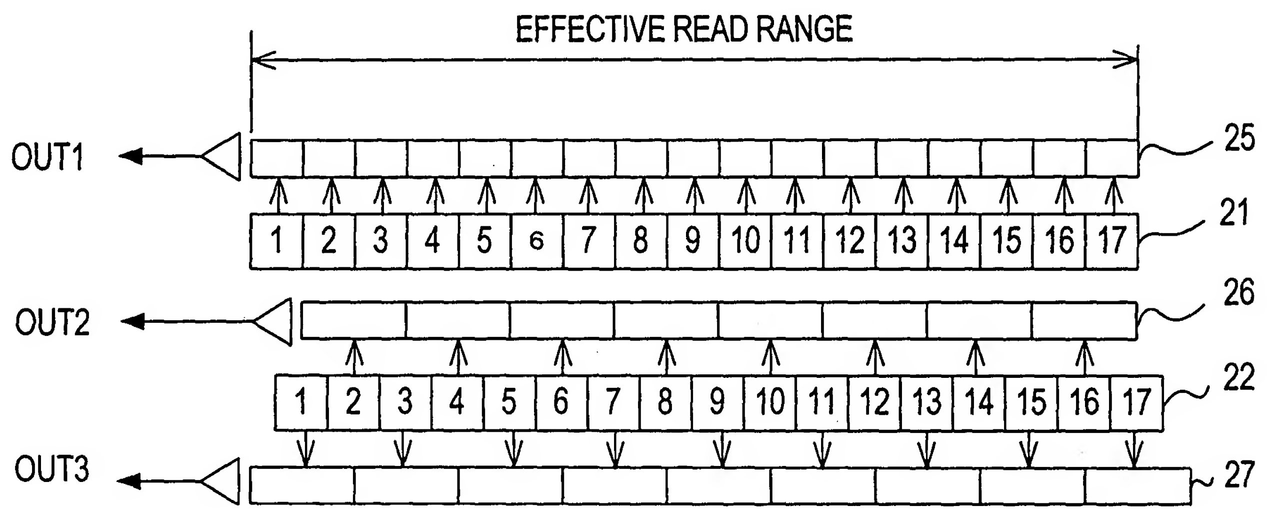
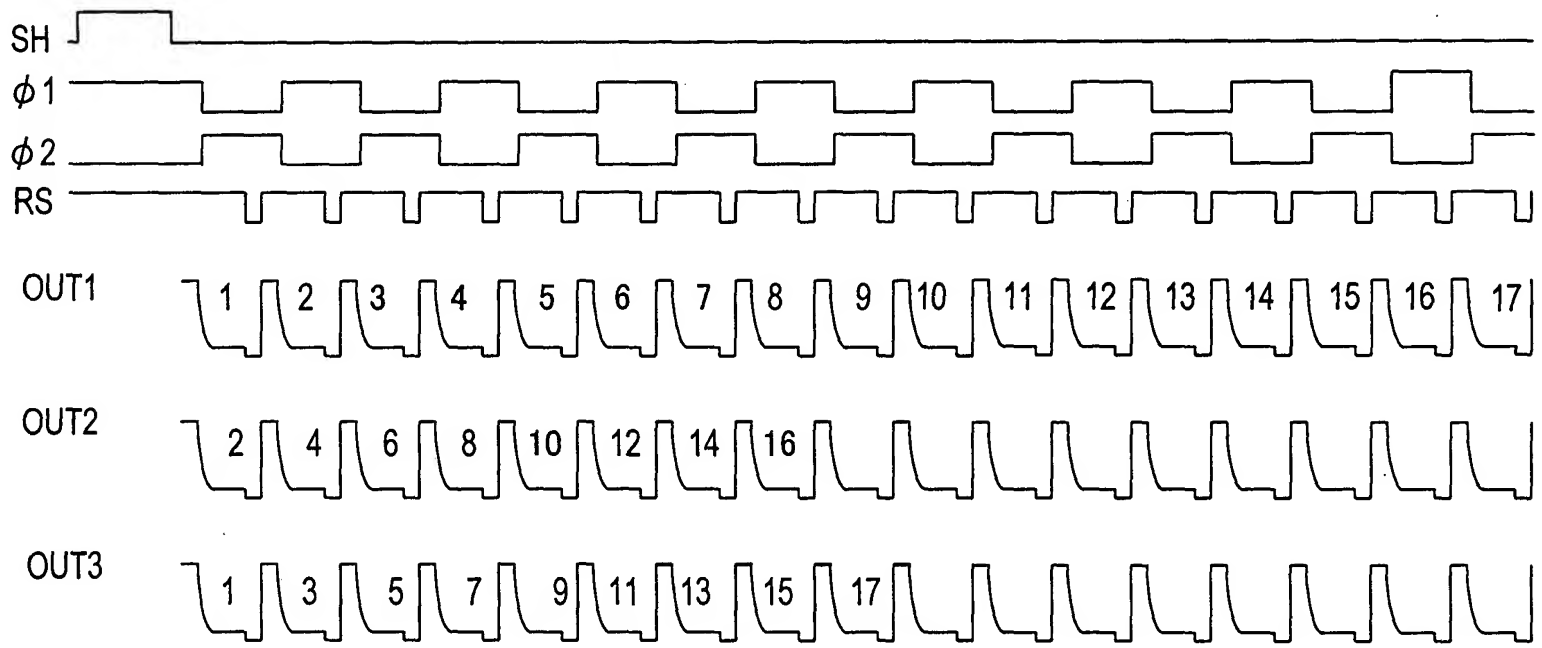

EFFECTIVE READ RANGE
OUT1
OUT2
OUT3
25
21
26
22
27
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17

FIG.3


SH
ϕ1
ϕ2
RS
OUT1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
OUT2
2
4
6
8
10
12
14
16
OUT3
1
3
5
7
9
11
13
15
17

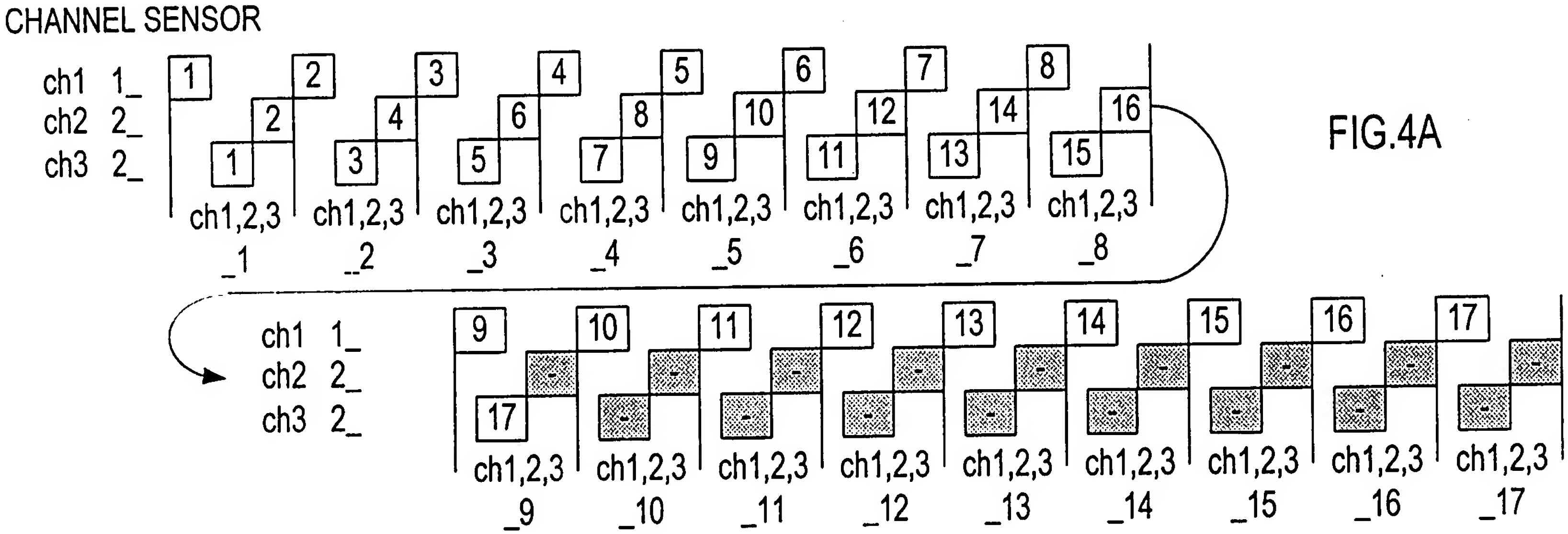

CHANNEL SENSOR
ch1 1_
ch2 2_
ch3 2_
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
ch1,2,3 _1
ch1,2,3 _2
ch1,2,3 _3
ch1,2,3 _4
ch1,2,3 _5
ch1,2,3 _6
ch1,2,3 _7
ch1,2,3 _8
ch1 1_
ch2 2_
ch3 2_
ch1,2,3 _9
ch1,2,3 _10
ch1,2,3 _11
ch1,2,3 _12
ch1,2,3 _13
ch1,2,3 _14
ch1,2,3 _15
ch1,2,3 _16
ch1,2,3 _17

FIG.4A

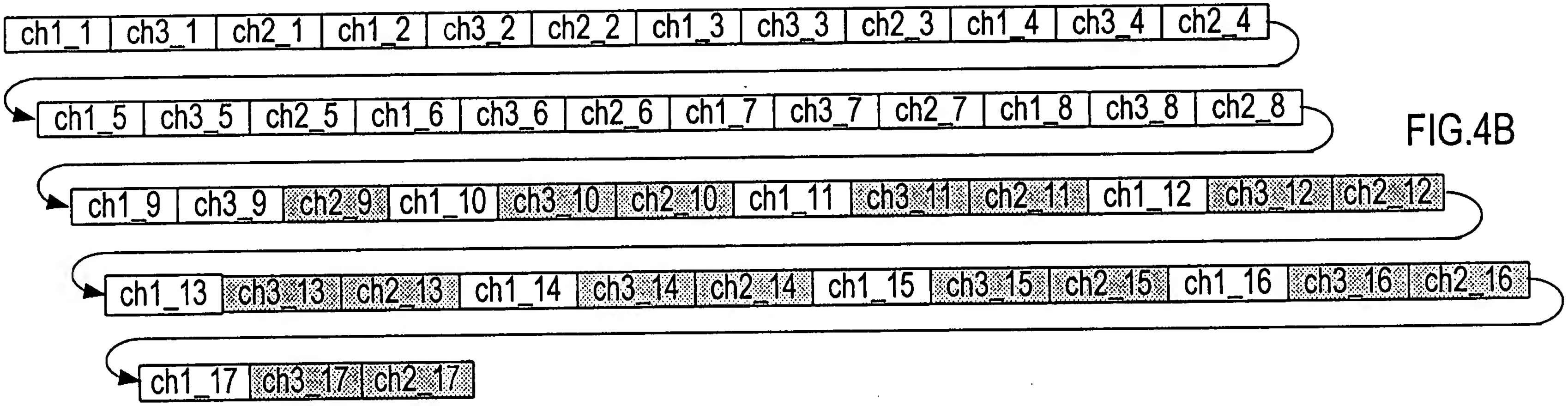

ch1_1
ch3_1
ch2_1
ch1_2
ch3_2
ch2_2
ch1_3
ch3_3
ch2_3
ch1_4
ch3_4
ch2_4
ch1_5
ch3_5
ch2_5
ch1_6
ch3_6
ch2_6
ch1_7
ch3_7
ch2_7
ch1_8
ch3_8
ch2_8
ch1_9
ch3_9
ch2_9
ch1_10
ch3_10
ch2_10
ch1_11
ch3_11
ch2_11
ch1_12
ch3_12
ch2_12
ch1_13
ch3_13
ch2_13
ch1_14
ch3_14
ch2_14
ch1_15
ch3_15
ch2_15
ch1_16
ch3_16
ch2_16
ch1_17
ch3_17
ch2_17

FIG.4B

FIG.5A

ch1_1	ch1_9	ch1_17
ch3_1	ch3_9	ch3_17
ch2_1	ch2_9	ch2_17
ch1_2	ch1_10	
ch3_2	ch3_10	
ch2_2	ch2_10	
ch1_3	ch1_11	
ch3_3	ch3_11	
ch2_3	ch2_11	
ch1_4	ch1_12	
ch3_4	ch3_12	
ch2_4	ch2_12	
ch1_5	ch1_13	
ch3_5	ch3_13	
ch2_5	ch2_13	
ch1_6	ch1_14	
ch3_6	ch3_14	
ch2_6	ch2_14	
ch1_7	ch1_15	
ch3_7	ch3_15	
ch2_7	ch2_15	
ch1_8	ch1_16	
ch3_8	ch3_16	
ch2_8	ch2_16	

FIG.5B

ch1_1	ch1_9	
ch3_1	ch3_9	
ch2_1	ch1_10	
ch1_2	ch1_11	
ch3_2	ch1_12	
ch2_2	ch1_13	
ch1_3	ch1_14	
ch3_3	ch1_15	
ch2_3	ch1_16	
ch1_4	ch1_17	
ch3_4		
ch2_4		
ch1_5		
ch3_5		
ch2_5		
ch1_6		
ch3_6		
ch2_6		
ch1_7		
ch3_7		
ch2_7		
ch1_8		
ch3_8		
ch2_8		

FIG.6

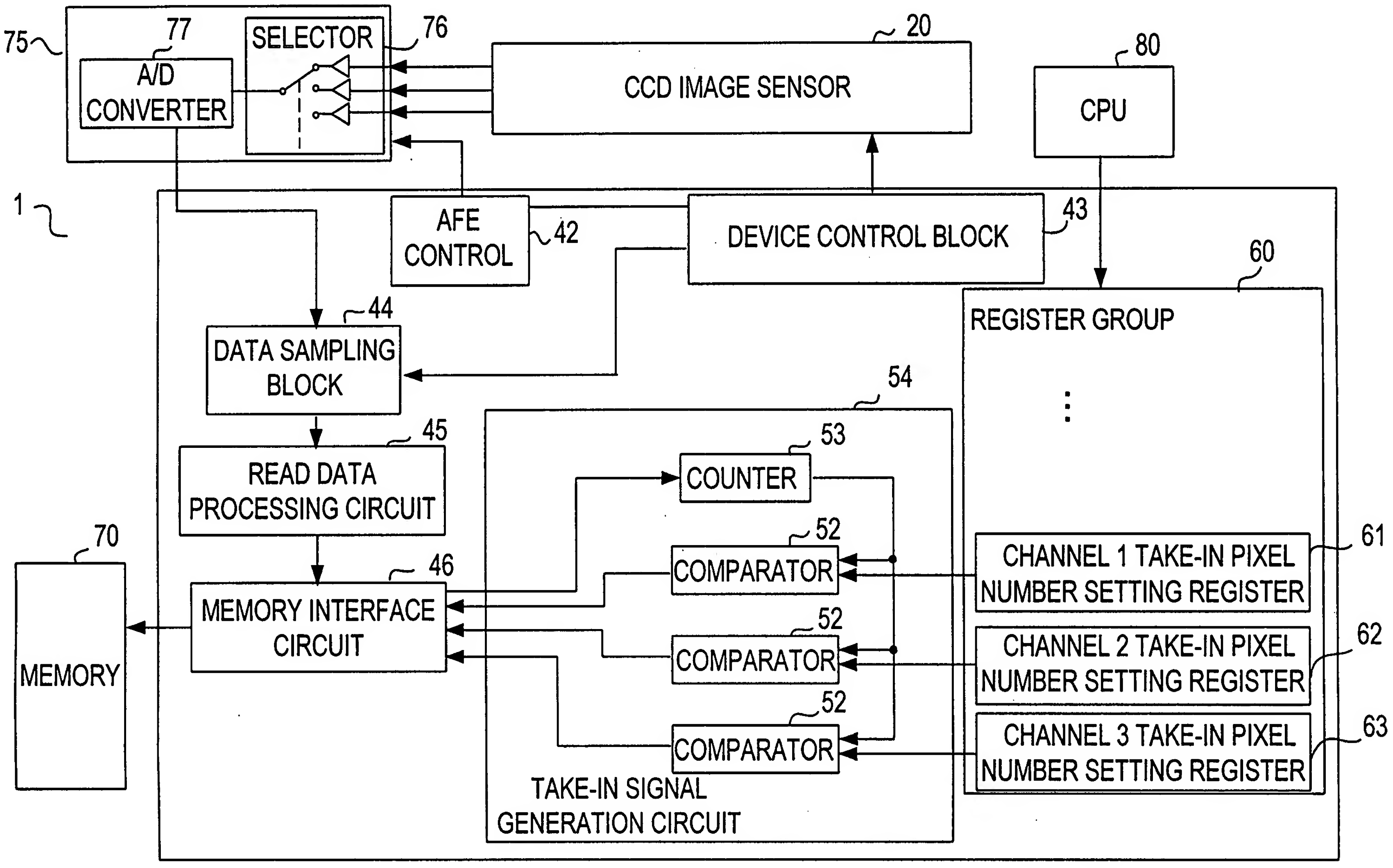

75
77
A/D CONVERTER
SELECTOR
76
CCD IMAGE SENSOR
20
CPU
80
1
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
60
REGISTER GROUP
...
44
DATA SAMPLING BLOCK
54
45
READ DATA PROCESSING CIRCUIT
53
COUNTER
70
52
COMPARATOR
MEMORY
46
MEMORY INTERFACE CIRCUIT
52
COMPARATOR
52
COMPARATOR
CHANNEL 1 TAKE-IN PIXEL NUMBER SETTING REGISTER
61
CHANNEL 2 TAKE-IN PIXEL NUMBER SETTING REGISTER
62
CHANNEL 3 TAKE-IN PIXEL NUMBER SETTING REGISTER
63
TAKE-IN SIGNAL GENERATION CIRCUIT

FIG.7

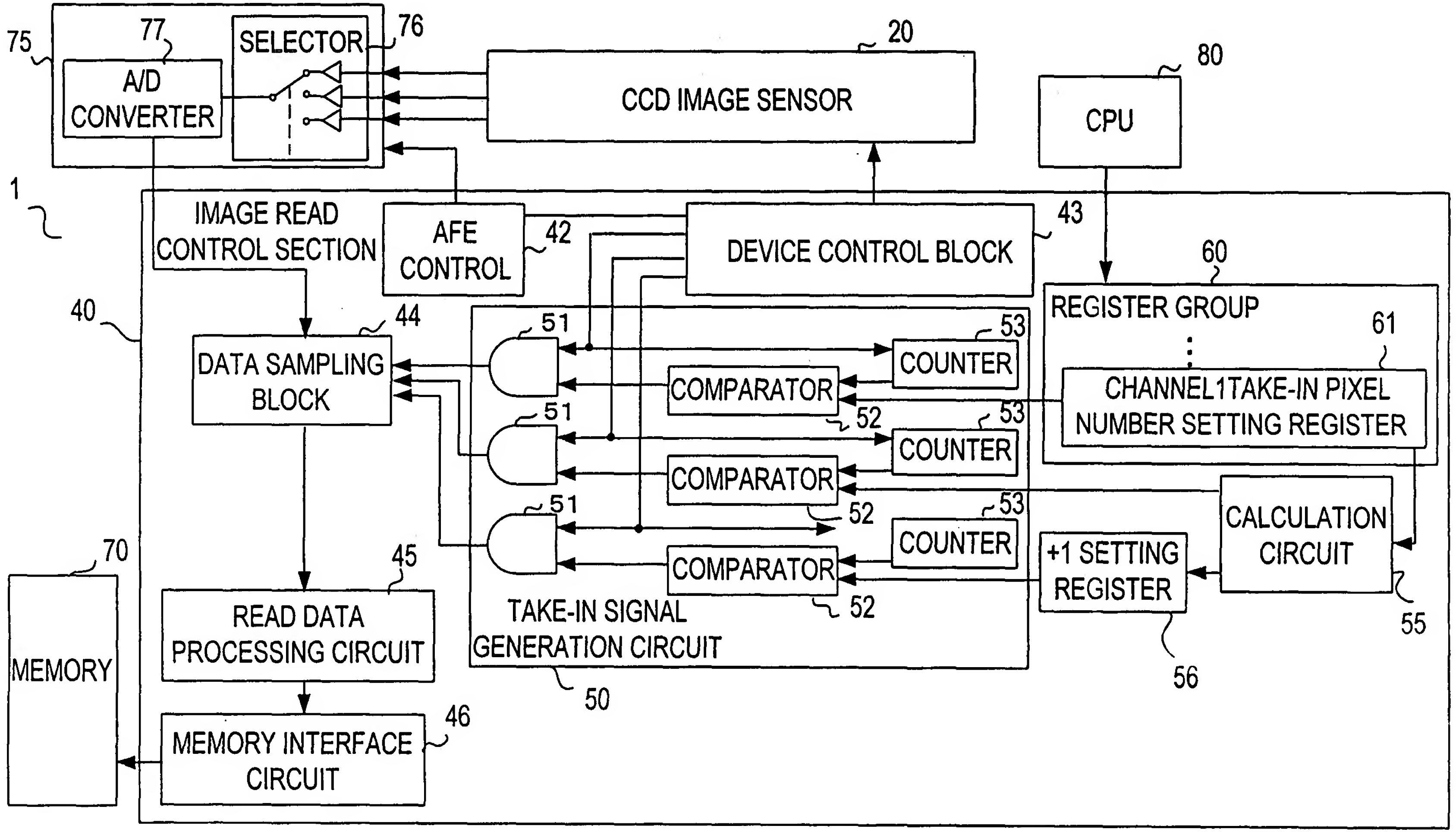
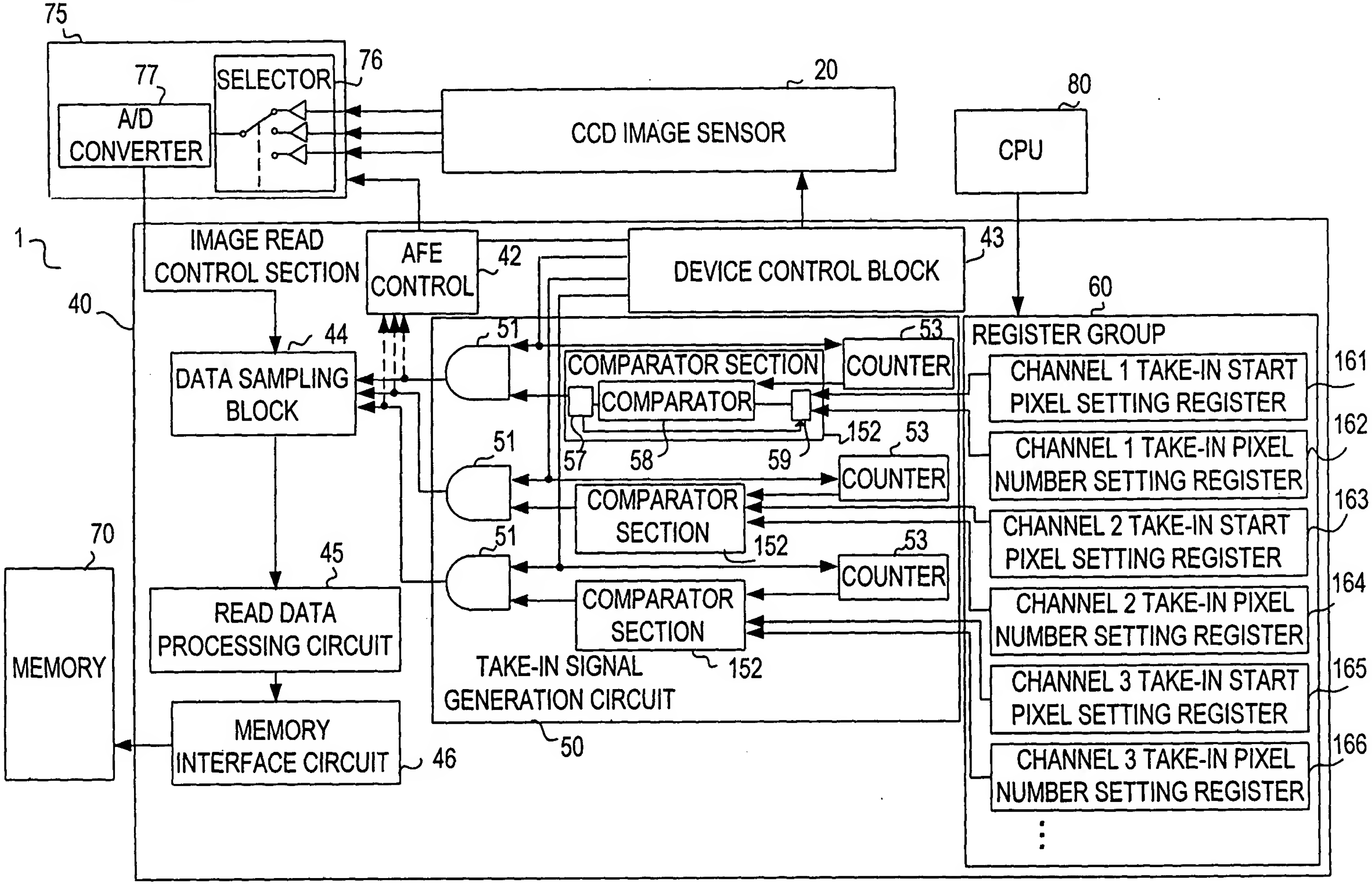
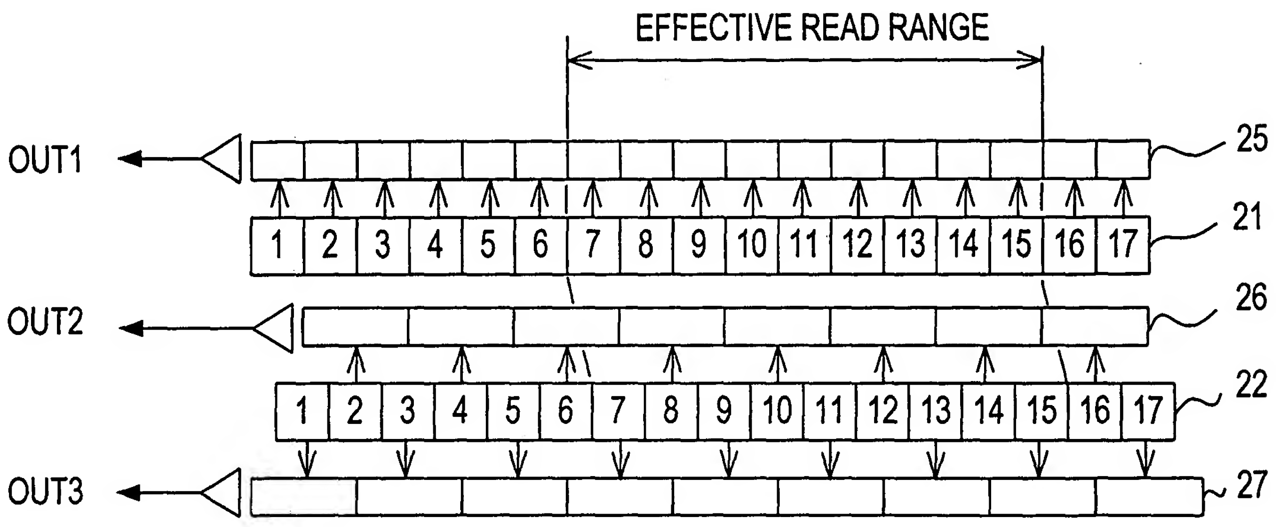

75
77
A/D CONVERTER
SELECTOR
76
20
CCD IMAGE SENSOR
80
CPU
1
IMAGE READ CONTROL SECTION
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
60
REGISTER GROUP
61
CHANNEL1TAKE-IN PIXEL NUMBER SETTING REGISTER
40
44
DATA SAMPLING BLOCK
51
53
COUNTER
COMPARATOR
52
51
53
COUNTER
COMPARATOR
52
51
53
COUNTER
COMPARATOR
52
CALCULATION CIRCUIT
+1 SETTING REGISTER
55
56
70
MEMORY
45
READ DATA PROCESSING CIRCUIT
TAKE-IN SIGNAL GENERATION CIRCUIT
50
46
MEMORY INTERFACE CIRCUIT

FIG.8



75
77
A/D CONVERTER
SELECTOR
76
CCD IMAGE SENSOR
20
CPU
80
1
40
IMAGE READ CONTROL SECTION
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
60
REGISTER GROUP
44
DATA SAMPLING BLOCK
51
51
51
COMPARATOR SECTION
COMPARATOR
57
58
59
152
COUNTER
53
53
53
COUNTER
COUNTER
COMPARATOR SECTION
152
COMPARATOR SECTION
152
CHANNEL 1 TAKE-IN START PIXEL SETTING REGISTER
161
CHANNEL 1 TAKE-IN PIXEL NUMBER SETTING REGISTER
162
CHANNEL 2 TAKE-IN START PIXEL SETTING REGISTER
163
CHANNEL 2 TAKE-IN PIXEL NUMBER SETTING REGISTER
164
CHANNEL 3 TAKE-IN START PIXEL SETTING REGISTER
165
CHANNEL 3 TAKE-IN PIXEL NUMBER SETTING REGISTER
166
70
MEMORY
45
READ DATA PROCESSING CIRCUIT
MEMORY INTERFACE CIRCUIT
46
TAKE-IN SIGNAL GENERATION CIRCUIT
50

FIG.9


EFFECTIVE READ RANGE
OUT1
OUT2
OUT3
25
21
26
22
27
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17

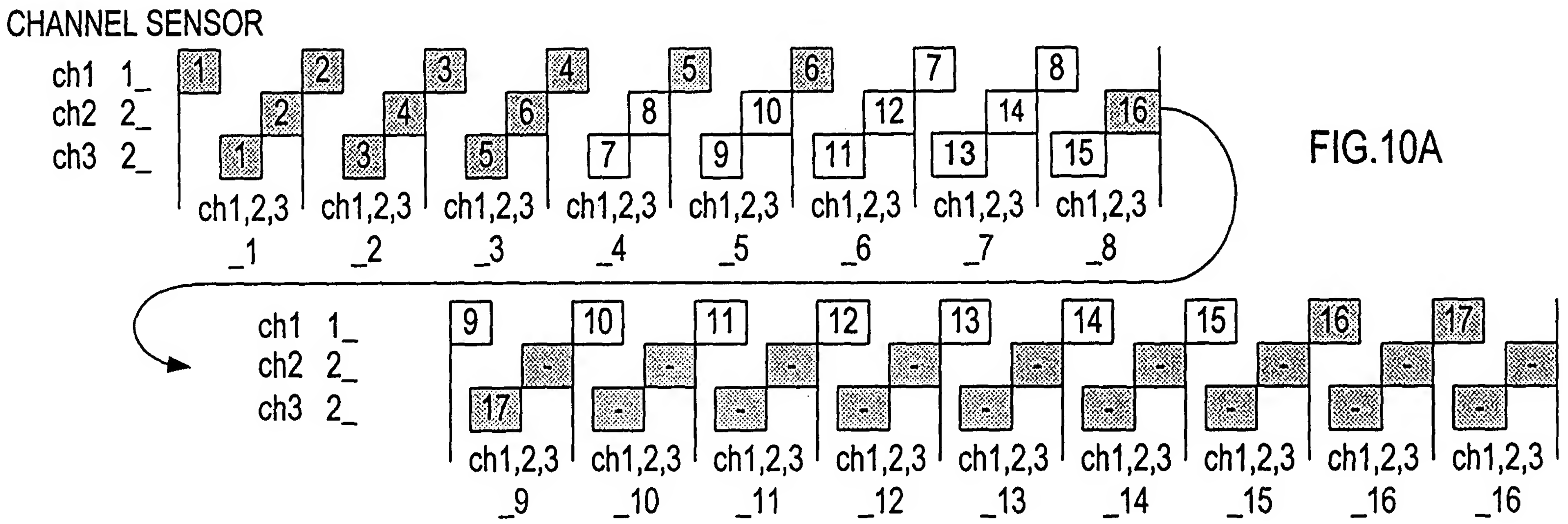


FIG.10A

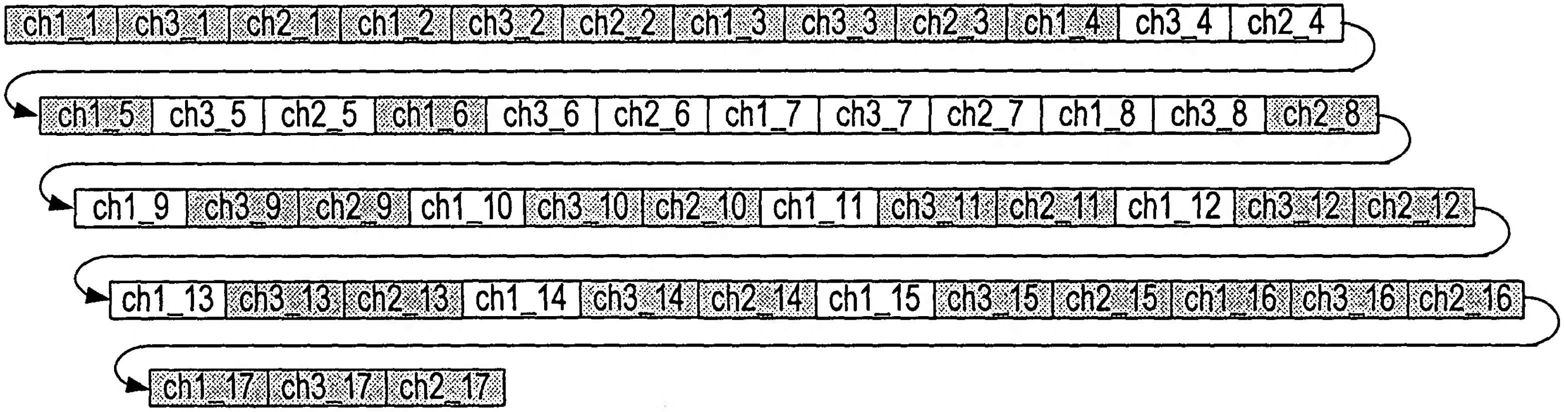
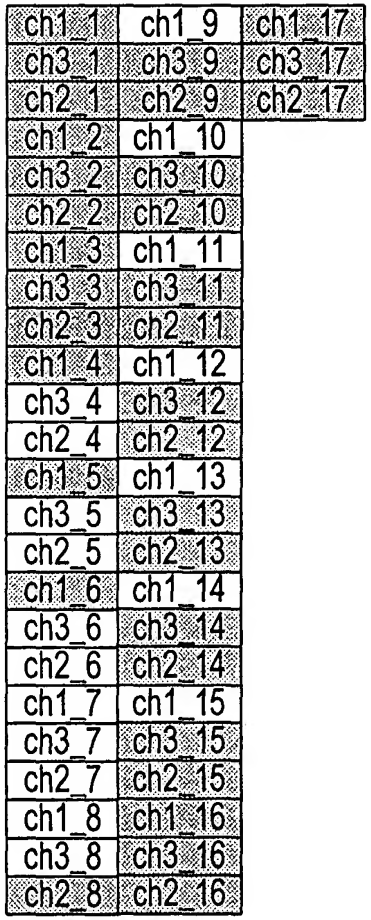


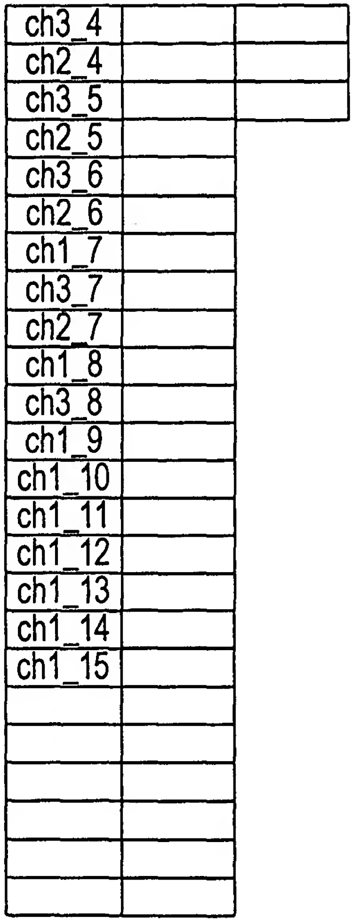
FIG.10B

FIG.11A



ch1_1	ch1_9	ch1_17
ch3_1	ch3_9	ch3_17
ch2_1	ch2_9	ch2_17
ch1_2	ch1_10	
ch3_2	ch3_10	
ch2_2	ch2_10	
ch1_3	ch1_11	
ch3_3	ch3_11	
ch2_3	ch2_11	
ch1_4	ch1_12	
ch3_4	ch3_12	
ch2_4	ch2_12	
ch1_5	ch1_13	
ch3_5	ch3_13	
ch2_5	ch2_13	
ch1_6	ch1_14	
ch3_6	ch3_14	
ch2_6	ch2_14	
ch1_7	ch1_15	
ch3_7	ch3_15	
ch2_7	ch2_15	
ch1_8	ch1_16	
ch3_8	ch3_16	
ch2_8	ch2_16	

FIG.11B



ch3_4		
ch2_4		
ch3_5		
ch2_5		
ch3_6		
ch2_6		
ch1_7		
ch3_7		
ch2_7		
ch1_8		
ch3_8		
ch1_9		
ch1_10		
ch1_11		
ch1_12		
ch1_13		
ch1_14		
ch1_15		

FIG.12

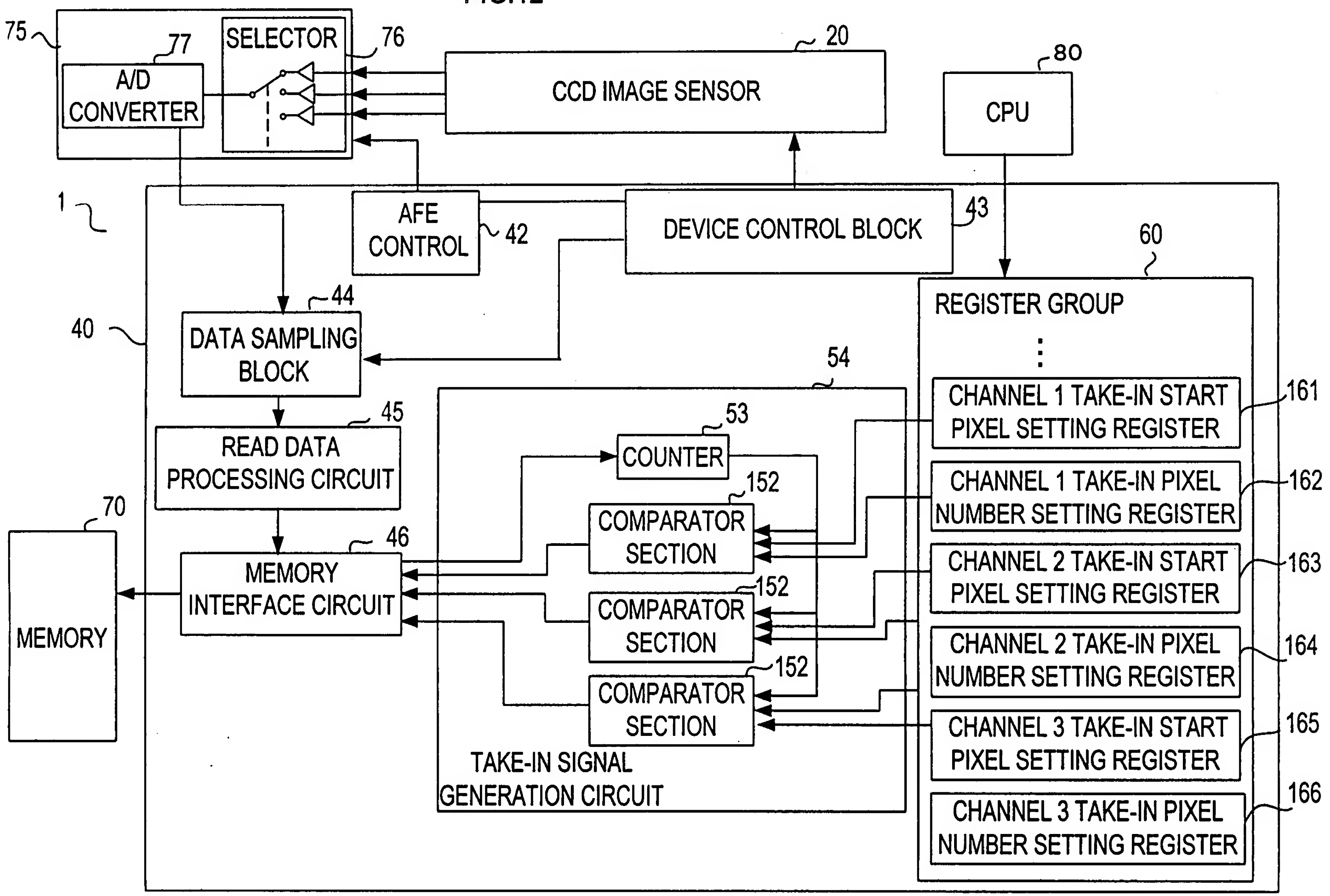

75
77
A/D CONVERTER
SELECTOR
76
20
CCD IMAGE SENSOR
80
CPU
1
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
60
40
44
DATA SAMPLING BLOCK
REGISTER GROUP
54
45
READ DATA PROCESSING CIRCUIT
53
COUNTER
CHANNEL 1 TAKE-IN START PIXEL SETTING REGISTER
161
CHANNEL 1 TAKE-IN PIXEL NUMBER SETTING REGISTER
162
70
MEMORY
46
MEMORY INTERFACE CIRCUIT
152
COMPARATOR SECTION
152
COMPARATOR SECTION
152
COMPARATOR SECTION
CHANNEL 2 TAKE-IN START PIXEL SETTING REGISTER
163
CHANNEL 2 TAKE-IN PIXEL NUMBER SETTING REGISTER
164
CHANNEL 3 TAKE-IN START PIXEL SETTING REGISTER
165
CHANNEL 3 TAKE-IN PIXEL NUMBER SETTING REGISTER
166
TAKE-IN SIGNAL GENERATION CIRCUIT

FIG.13

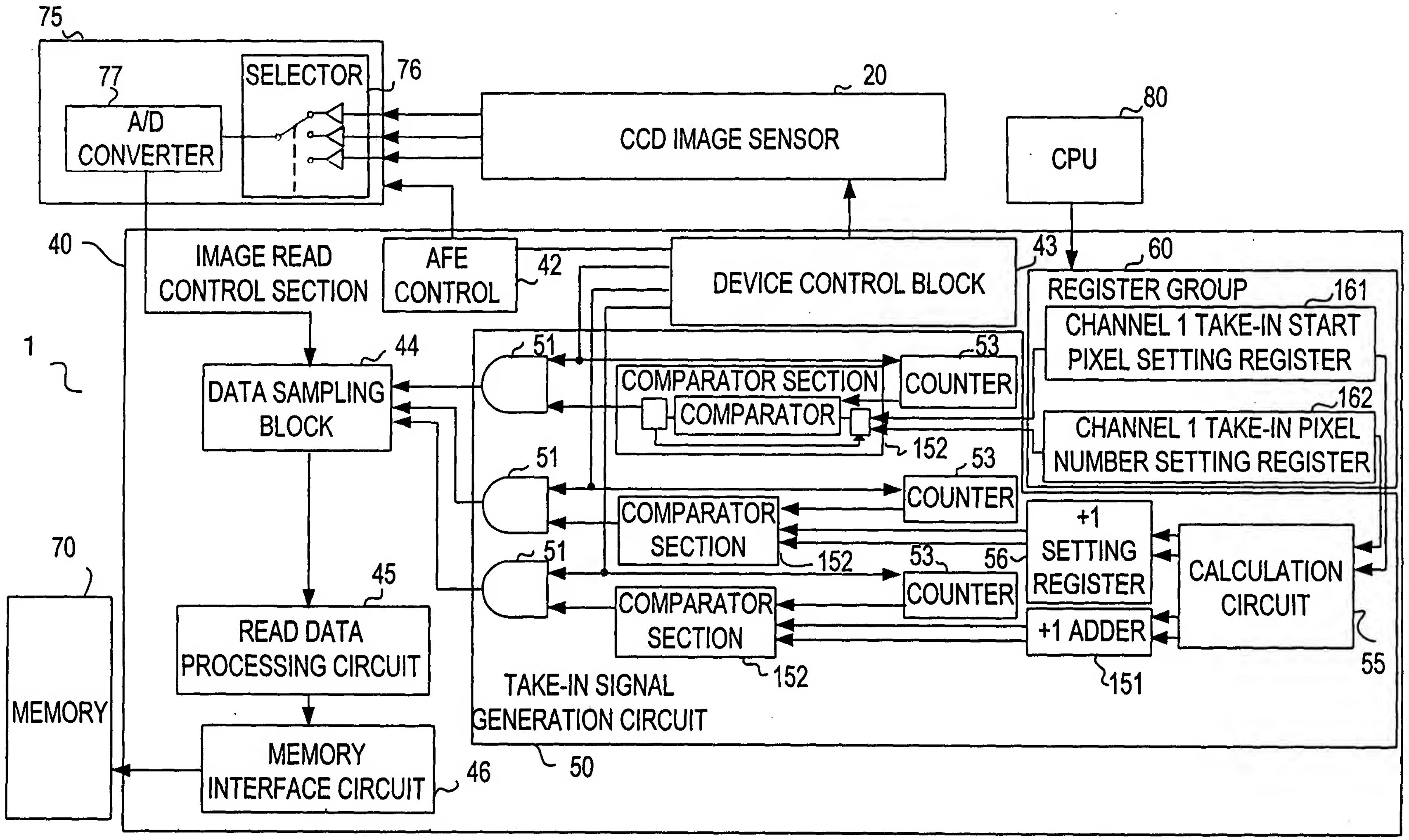

75
77
A/D CONVERTER
SELECTOR
76
20
CCD IMAGE SENSOR
80
CPU
40
IMAGE READ CONTROL SECTION
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
60
REGISTER GROUP
161
CHANNEL 1 TAKE-IN START PIXEL SETTING REGISTER
162
CHANNEL 1 TAKE-IN PIXEL NUMBER SETTING REGISTER
1
44
DATA SAMPLING BLOCK
51
51
51
COMPARATOR SECTION
COMPARATOR
152
53
COUNTER
53
COUNTER
COMPARATOR SECTION
152
53
COUNTER
56
+1 SETTING REGISTER
CALCULATION CIRCUIT
55
COMPARATOR SECTION
152
+1 ADDER
151
70
MEMORY
45
READ DATA PROCESSING CIRCUIT
MEMORY INTERFACE CIRCUIT
46
TAKE-IN SIGNAL GENERATION CIRCUIT
50

FIG.14

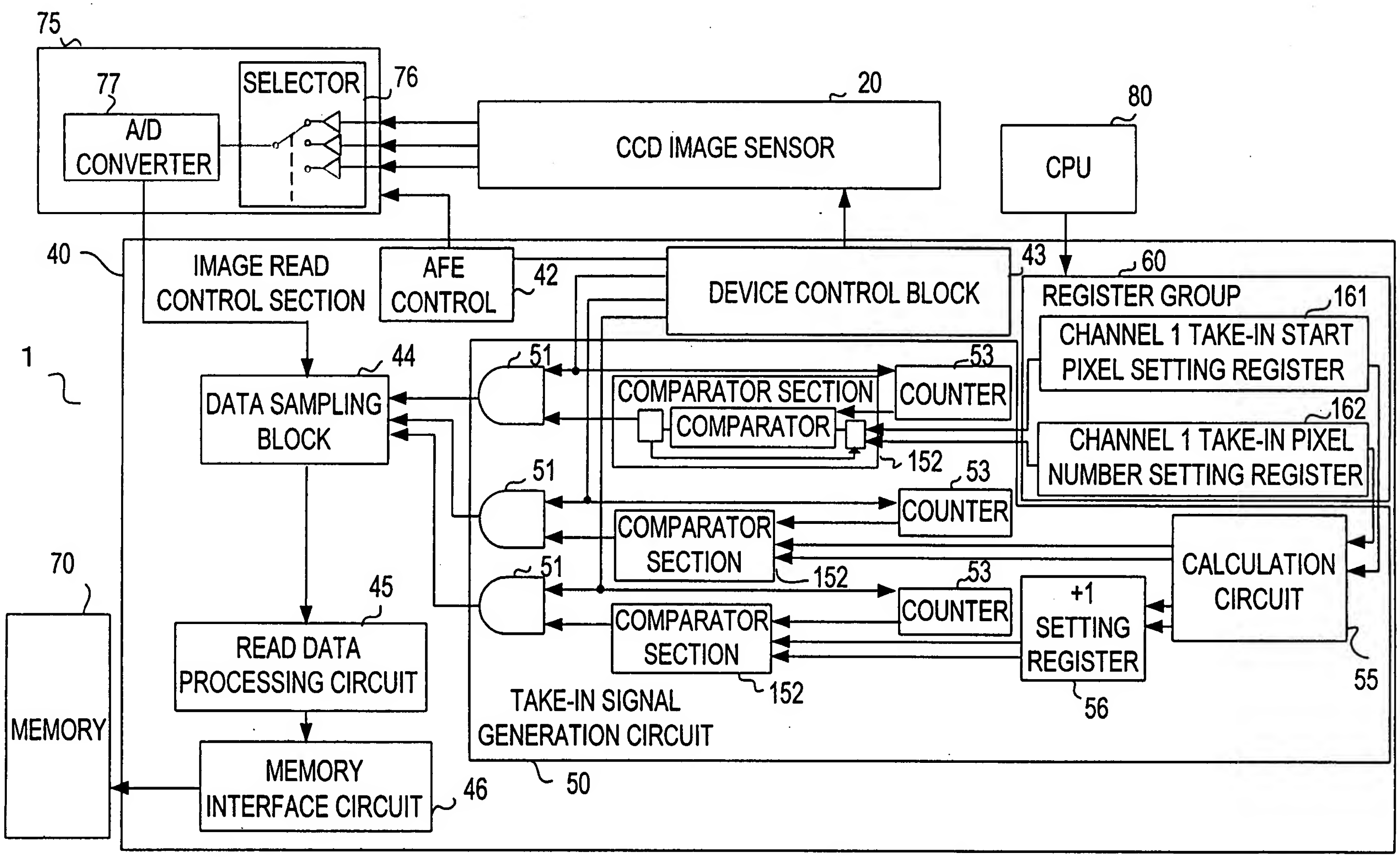
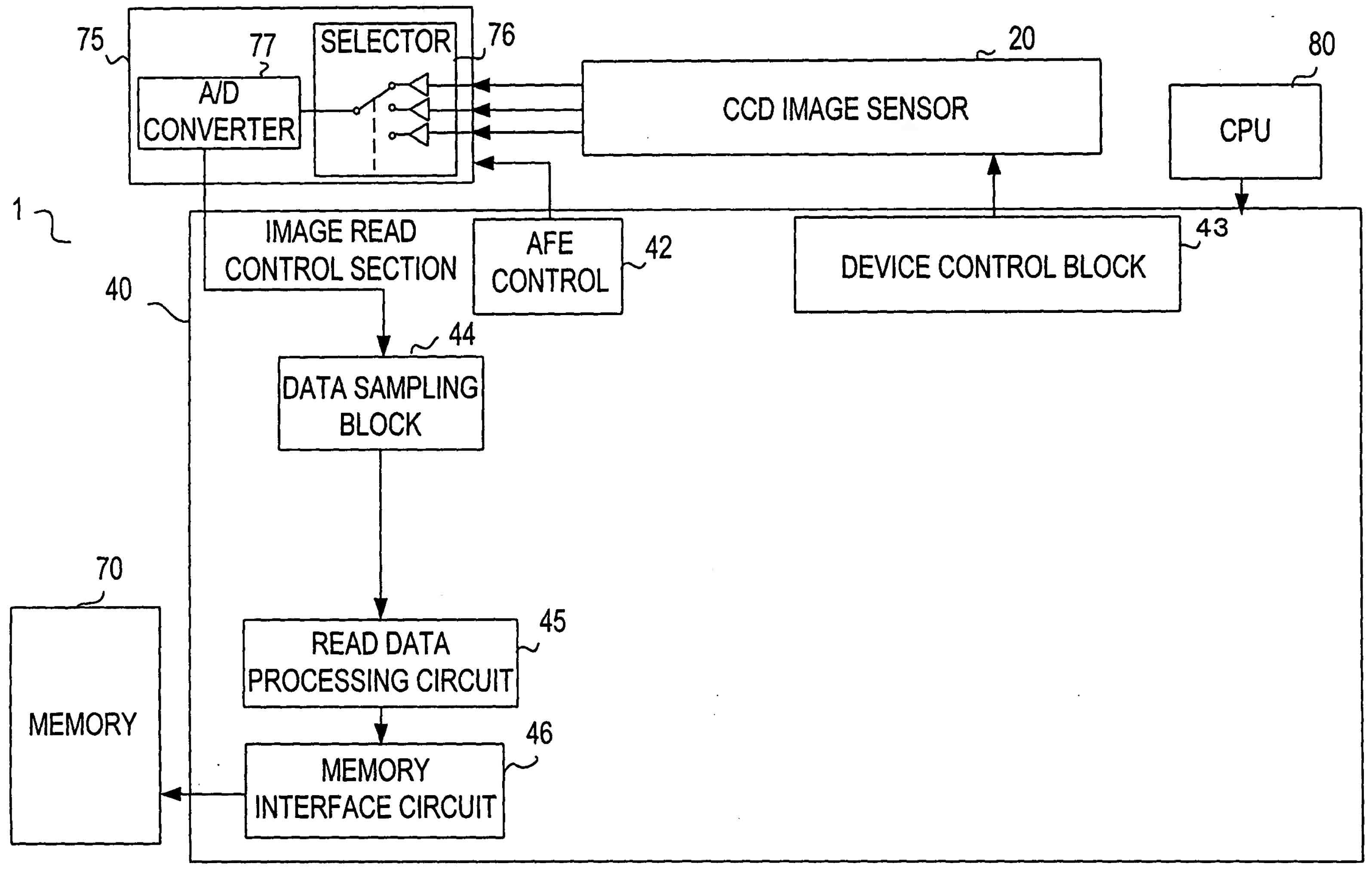

75
77
A/D CONVERTER
SELECTOR
76
20
CCD IMAGE SENSOR
80
CPU
40
IMAGE READ CONTROL SECTION
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
60
REGISTER GROUP
161
CHANNEL 1 TAKE-IN START PIXEL SETTING REGISTER
162
CHANNEL 1 TAKE-IN PIXEL NUMBER SETTING REGISTER
1
44
DATA SAMPLING BLOCK
51
51
51
COMPARATOR SECTION
COMPARATOR
152
53
COUNTER
53
COUNTER
53
COUNTER
COMPARATOR SECTION
152
COMPARATOR SECTION
152
CALCULATION CIRCUIT
55
+1 SETTING REGISTER
56
70
MEMORY
45
READ DATA PROCESSING CIRCUIT
MEMORY INTERFACE CIRCUIT
46
TAKE-IN SIGNAL GENERATION CIRCUIT
50

FIG.15


75
77
A/D CONVERTER
SELECTOR
76
20
CCD IMAGE SENSOR
80
CPU
1
40
IMAGE READ CONTROL SECTION
AFE CONTROL
42
DEVICE CONTROL BLOCK
43
44
DATA SAMPLING BLOCK
70
MEMORY
READ DATA PROCESSING CIRCUIT
45
MEMORY INTERFACE CIRCUIT
46